

RFL Electronics, Inc.

DACS / ILS Application Note 05.

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IMUX 2000

DACS

CLOCK SELECTION

The DACS module of the RFL IMUX 2000 system can be configured to utilize various sources for its internal system clock.

The system clock drives the internal DS0 grooming process and serves as the T1 transmit clock. External clock and/or any of the 6 ports and/or the internal oscillator can serve as a clock source. One or two sources can be selected.

When using the SCL commands or RFL Network Management System, the following choices are available:

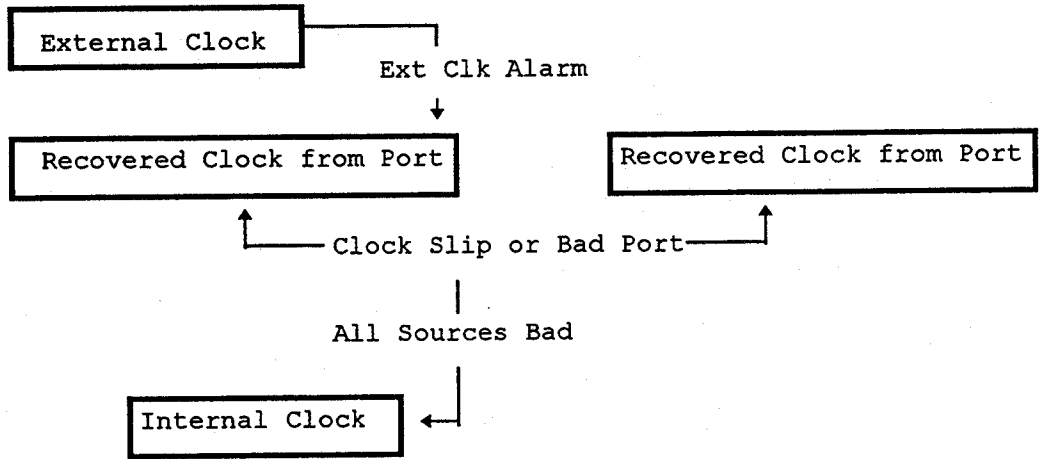
CLOCK values: [primary],[alternate] DACS primary and alternate clock source where [primary] or [alternate] = [1..6], [M1..M6], INT, EXT, NONE

SCL example: node:dacs:set:clock=ext,4;
selects external clock to drive the system, with clock recovered from port 4 as the alternate.

CLOCK HIERARCHY.

Internal clock, even if not selected directly on the command line, will be used if none of the selected clock sources are available.

External clock, if present and if enabled by CLOCK parameter, takes precedence over any other sources. This means that regardless of any other sources, the DACS processor will attempt to switch into the external source.



Clock source hierarchy.

If a problem is detected at the current source of clock, DACS will use the alternate source. If the problem clears, DACS will not attempt to switch back unless there is a problem with the alternate.

If clock slippage is detected, the processor will switch between port sources specified in CLOCK parameter.

If the current source is external and it is specified in CLOCK, the above does not apply. DACS will never attempt to switch out of external and will ignore any slips between external and other clocks.

CLOCK SWITCH SEQUENCE.

The clock switching circuit has been carefully designed to provide a smooth transition between the sources. The source cannot be switched at a random instance, since this would result in a distorted clock "tick" and possibly in an extra clock pulse, thus disturbing the data flow throughout the whole network. Such a disturbance could have quite serious consequences.

When a source switch is attempted, the selector circuit waits until the currently used clock "slides" past the new, requested clock until both clocks coincide at the same edge. Then, and only then, the new clock will seamlessly take over.

There are only 2 exceptions to this rule. Clocks are set up asynchronously during the power-up initialization sequence, for obvious reasons. Also, if the external clock fails while it is being used, the system will be forced to the alternate selection or to the internal oscillator at once, since the alternate cannot "slide" smoothly past a non-existent external clock. However, if the external clock is re-established, the system will wait until the external clock precisely aligns with the currently used clock before it switches back to external.

The requirement that sources must coincide in order to switch clocks results in the fact the DACS may not necessarily switch to clock specified in the clock parameter, if that is identical to the one currently used.

For example, consider a situation where a DACS is being set by a user to `clock=4`; , while it is currently using port 1 for its source. If the clocks recovered from ports 4 and 1 are identical to the point where their edges do not move past each other, the DACS will continue using port 1. Only a slip of these clocks past each other will result in the switch of sources.

The actual sequence of switching proceeds as follows:

- One of the clocks specified in the CLOCK parameter is used as the current system clock. The clock from the other source, if specified, is compared against the currently used clock in order to detect any slips.
- If the currently used clock is recovered from a port, and that port fails, the processor attempts to switch to the other source (or internal, if no other is specified). DACS waits for the now free-running recovered clock to slide past the requested clock and at that instance smoothly transitions into it. After the failed port is restored, the processor will use that port's clock for slippage reference, but will not switch back until another problem occurs.

- As mentioned above, if the currently used clock is external and it fails, the DACS abruptly forces its system clock to be sourced from the alternate source (or internal). After the failed external source is restored, the processor will attempt to switch back. That switch will occur only when the currently used clock slips past the external, in order to assure a smooth transition.
- If the currently used and the alternate clocks are recovered from ports (rather than external/internal), and 2 consecutive slips in the same direction between these clocks are detected without a failure of the associated ports, the processor determines that a fault occurred elsewhere in the network and attempts to switch to the other source. DACS waits until the currently used clock slides past the requested alternate clock and smoothly transitions into it. As the network re-arranges the clocks in response to a fault, several back-and-forth clock swaps may occur until everything settles.

ALTERNATE MASTER.

The M qualifier is used to compensate for the loss of master timing node in the system by setting up a secondary master.

In the next node "downstream" after the master, the port facing the master should be denoted as M. For example, if port 1 in next node after master is facing the master, the following command may be issued:

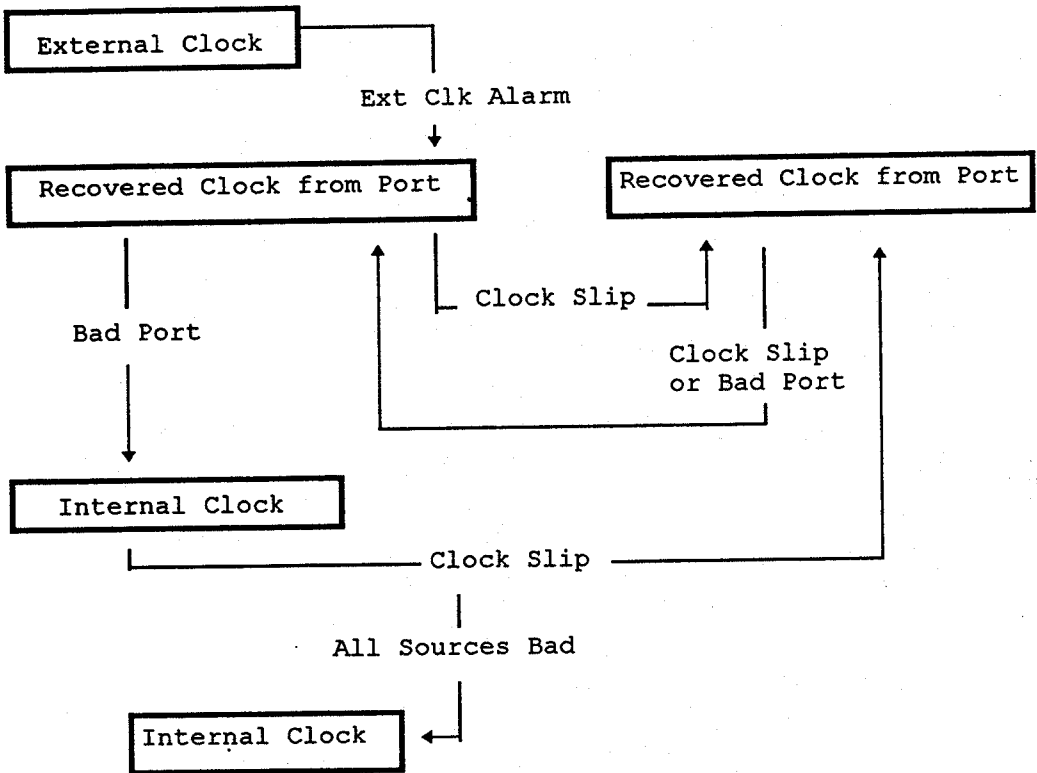
```
node:dacs:set:clock=M1,4;
```

Such command results in following sequence of events:

- If a failure is detected at port 1, the clock is first sourced from internal oscillator, regardless of what the other alternate source is. The processor will monitor the alternate source for clock slippage.
- If no slip is present, the processor assumes that its own clock propagated through the system. This indicates that master node is lost. The processor will remain in internal timing, assuming the function of a secondary master, until clock slip occurs.
- If clock slip occurs, then the processor knows that another source of timing is present in the system. DACS will switch to the alternate source specified in CLOCK parameter.

Note that only a port and only one port can be selected as M.

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Clock source hierarchy for secondary master.